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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,292	01/21/2004	Naofumi Ohashi	501.37370CC4	9846

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EXAMINER	
NGUYEN, HA T	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,292	OHASHI ET AL.	
	Examiner	Art Unit	
	Ha T. Nguyen	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 2-21 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 2-21 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 21 January 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 01-21-04,07-29-04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC. § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103 and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 2-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Edelstein et al. (USPN 6153043, hereinafter "Edelstein") in view of Hideaki (Hei 7-135192).

Referring to Figs. 1-4 and related text, Edelstein discloses [Re claim 2] a process for manufacturing a semiconductor integrated circuit device, comprising the steps of: (a) forming a metal layer including copper as its principal component over an insulating film over a first major surface of a wafer, the insulating film having a wiring groove pattern; (b) removing the metal layer outside the wiring groove pattern by a chemical mechanical polishing method so as to leave the metal layer in the wiring groove pattern, said removing being performed in a chemical mechanical polishing section of a single wafer processing apparatus; (c) after step (b), transferring the wafer to a post cleaning section of the wafer processing apparatus; (d) performing scrub or brush cleaning to the first major surface of the wafer with a liquid chemical or pure water in the post cleaning section; and (e) after step (d), making the first major surface of the wafer dry, wherein the single wafer processing apparatus has a light shielding structure

enclosing the post cleaning section; [Re claims 4 and 9] wherein the metal layer left in the wiring groove pattern in step (b) constitutes a portion of a metal wiring of a dual damascene wiring; [Re claim 8] wherein step (a) includes the substep of: (i) forming the metal layer including copper as its principal component over an upper surface of the insulating film and inside the wiring groove pattern; [Re claim 9] wherein the metal layer left in the wiring groove pattern in step (b) constitutes a portion of a metal wiring of a dual damascene wiring; [Re claim 10] wherein the first major surface of the wafer is kept wet from the end of step (b) to the end of step (d); [Re claims 11-12] wherein the light shielding structure includes a light shielding sheet (See col. 6, lines 34-57). But it fails to disclose expressly transferring the wafer while keeping the first major surface of the wafer wet with moving water and the light shielding structure is between the chemical mechanical polishing section and the post cleaning section. However, the missing limitations are well known in the art because Hideaki discloses the use of wet wafer transfer; [Re claim 3] wherein the moving water is a water shower; [Re claim 5] wherein step (d) is performed prior to a substantial progress of corrosion of the metal layer left in the wiring groove pattern.; [Re claim 6] wherein the first major surface of the wafer is kept wet from the end of step (b) to the end of step (d); [Re claim 7] wherein the moving water is a pure water shower (see page 12, 2nd full par.-p. 14). The combined teaching of Edelstein and Hideaki does not discloses the metal layer is deposited by electroplating and the light shielding structure is between the chemical mechanical polishing section and the post cleaning section. However, the examiner takes Official Notice that it is well known in the art that Cu is deposited by electroplating to reduce cost and improve metal quality. Besides, since the negative effect of light happens mainly in the post cleaning step since during CMP the wafer is hidden from light by the polishing pad and wafer holder, it would have been obvious to not enclose the mechanical polishing section within the shielding structure, in other words the shielding structure is between the chemical mechanical polishing section and the post cleaning section. A person of ordinary skill is motivated to modify Edelstein with Hideaki to obtain device with wiring of better quality and reliability.

[Re claim 13] The combined teaching of Edelstein and Hideaki discloses process for manufacturing a semiconductor integrated circuit device, comprising the steps of: (a) forming a metal layer over an insulating film over a first major surface of a wafer, the insulating film having first and second wiring groove patterns; (b) removing the metal layer outside the first and

second wiring groove patterns by a chemical mechanical polishing method so as to leave the metal layer in the first and second wiring groove patterns and thereby electrically dividing metal wiring members inside the first and second wiring groove patterns, said removing being performed in a chemical mechanical polishing section of a single wafer processing apparatus; (c) after step (b), transferring the wafer to a post cleaning section of the single wafer processing apparatus, while keeping the first major surface of the wafer wet with moving water; (d) performing scrub or brush cleaning to the first major surface of the wafer with a liquid chemical or pure water in the post cleaning section; and (e) after step (d), making the first major surface of the wafer dry, wherein the single wafer processing apparatus has a light shielding structure enclosing the post cleaning section and between the chemical mechanical polishing section and the post cleaning section; [Re claim 14] wherein the moving water is a water shower; [Re claim 15] wherein portions of the metal layer left inside the first and second wiring groove patterns in step (b) constitute portions of metal wiring members of a dual damascene wiring; [Re claims 16 and 20] wherein step (d) is performed prior to a substantial progress of corrosion of the metal layer left in the first and second wiring groove patterns;[Re claims 17 and 21] wherein the first major surface of the wafer is kept wet from the end of step (b) to the end of step (d);[Re claim 18] wherein the moving water is a pure water shower; [Re claim 19] wherein portions of the metal layer left inside the first and second wiring groove patterns in step (b) constitute portions of metal wiring members of a dual damascene wiring, as shown above.

Therefore, it would have been obvious to combine Edelstein with Hideaki to obtain the invention as specified in claims 2-21 .

Double Patenting Rejection

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686

F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 2-6 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1,1-4, respectively, of U.S. Patent No 6531 400. Although the conflicting claims are not identical, they are not patentably distinct from each other because are broader in scope than the claims 1, 1-4 of the patent.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ha T. Nguyen whose telephone number is (571) 272-1678. The examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM, except the first Friday of each bi-week. The telephone number for Wednesday is (703) 560-0528.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt, can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ha Nguyen

Primary Examiner

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